

[0131] The processor 2200 may perform calculations or tasks. According to an exemplary embodiment, the processor 2200 may be a microprocessor or a central processing unit (CPU). The processor 2200 may communicate with the RAM 2300, the input/output device 2400, and the memory system 2100 through a bus 2600 such as an address bus, a control bus, or a data bus. According to an exemplary embodiment, the processor 2200 may be connected to an extension bus such as a peripheral component interconnect (PCI) bus. According to exemplary embodiments described above, the memory system 2100 may include memory 2110, be managed by the processor 2200 and operated by a memory controller 2120.

[0132] The RAM 2300 may store data for an operation of the computing system 2000. For example, the RAM 2300 may be realized as dynamic random access memory (DRAM), mobile DRAM, static RAM (SRAM), PRAM, ferroelectrics RAM (FRAM), RRAM and/or MRAM. The input/output device 2400 may include an input interface, such as a keyboard, a keypad, or a mouse, and an output interface, such as a printer or a display. The power supply 2500 may supply an operating voltage for the computing system 2000.

[0133] FIG. 21 is a block diagram of a system 3000 including an SSD (solid state drive or solid disk device) 3200, according to various exemplary embodiments. Referring to FIG. 21, the system 3000 may include a host 3100 and the SSD 3200. The SSD 3200 exchanges a signal with the host 3100 through a signal connector, and receives power through a power connector. The SSD 3200 may include an SSD controller 3210, an auxiliary power supply 3220, and a plurality of memory devices 3230, 3240, and 3250 connected to the SSD controller 3210 via channels Ch1 through Chn. According to exemplary embodiments described above, the SSD 3200 may be managed by the host 3100 and operated by the SSD controller 3210.

[0134] While the inventive concept has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

What is claimed is:

1. A method of operating a storage device in communication with a host, the method comprising:

receiving a first target value and a second target value of a plurality of target values respectively corresponding to a first operating parameter and a second operating parameter of a plurality of operating parameters of the storage device from the host;

loading a first existing value and a second existing value of a plurality of existing values of the first operating parameter and the second operating parameter;

processing a machine learning algorithm using the first target value, the second target value, the first existing value and the second existing value to generate an adaptive schedule;

adaptively scheduling a background operation of the storage device based on the generated adaptive schedule; and

executing the background operation based on the adaptive scheduling of the background operation.

2. The method of claim 1, wherein

the first operating parameter corresponds to a state of the storage device, and

the loading of existing values of the operating parameters comprises measuring or calculating the state of the storage device.

3. The method of claim 2, wherein

the first operating parameter comprises at least one among a number of free blocks of the storage device, a wear level index, a temperature, a rate of internal operation, and an error correction time.

4. The method of claim 1, wherein

the second operating parameter corresponds to a state of the host, and

the loading of existing values of the operating parameters comprises receiving the second operating parameter from the host.

5. The method of claim 4, wherein

the second operating parameter comprises at least one among an input/output throughput, an input/output latency, a load index, an estimated idle time, and an estimated input/output usage.

6. The method of claim 1, wherein

the machine learning algorithm is a Q-learning algorithm.

7. The method of claim 6, further comprising:

calculating a performance score proportional to an absolute value of the difference between the target values and the existing values using the Q-learning algorithm; and

determining a timing label corresponding to a row comprising the highest Q value in a table comprised of rows of combinations of the operating parameters and columns of timing information of the background operation,

wherein the adaptive scheduling of the background operation is based on the determined timing label.

8. The method of claim 1, wherein

the storage device comprises a flash memory device, and the background operation is a garbage collection operation corresponding to the flash memory device.

9. The method of claim 1, wherein the machine learning algorithm is processed using the first target value, the second target value, the first existing value, the second existing value, a first weight of the first operating parameter and a second weight of the second operating parameter.

10. A method of managing a storage device by a host in communication with the storage device, the method comprising:

setting a first target value and a second target value of a plurality of target values respectively corresponding to a first operating parameter and a second operating parameter of a plurality of operating parameters of the storage device;

loading a first existing value and a second existing value of a plurality of existing values of the first operating parameter and the second operating parameter;

processing a machine learning algorithm using the first target value, the second target value, the first existing value and the second existing value to generate an adaptive schedule;

adaptively scheduling a background operation of the storage device based on the generated adaptive schedule;

generating a control signal to control the storage device to execute the background operation based on the adaptive scheduling of the background operation; and transmitting the control signal to the storage device.